POWER MOSFET HAVING A DRAIN **HETEROJUNCTION**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a field effect transistor and, more particularly, provides a technology directed toward lowering the on-resistance of a power MOSFET having a high breakdown voltage.

2. Description of the Prior Art

As a lateral power MOSFET in the prior art, a structure shown in FIG. 1, for example, has been known. In FIG. 1, a high impurity concentration n+-type Si buried layer 3 is formed between a p-type silicon (abbreviated as "Si" 15 hereinafter) substrate 1 and a p-type Si epitaxial layer 2. An n-type Si drain region 4 is formed in the p-type Si epitaxial layer 2 to be connected to the high impurity concentration n⁺-type Si buried layer 3. P-type Si base regions (channel regions) 5 and a high impurity concentration n⁺-type Si drain 20 region 18 are formed in the n-type Si drain region 4. High impurity concentration n⁺-type Si source regions 6 are formed in the p-type Si base region 5. A gate electrode 11 made of polysilicon is formed on the p type Si base region 5 and a part of the n-type Si drain region 4 via a gate oxide 25 film 7. In addition, a source electrode 12 is formed to be isolated from the gate electrode 11 by a first interlayer film 9. A drain electrode 13 is formed to be isolated from the source electrode 12 by a second interlayer film 10.

predetermined potential, e.g., a positive potential is applied to the gate electrode 11 under the condition that a voltage is applied between the drain electrode 13 and the source electrode 12, an n-type inversion layer is formed on a surface of the p-type Si base region 5 immediately below the 35 gate electrode 11 so that a drain current is passed from the drain electrode 13 to the source electrode 12. Conversely, if either 0 V or another predetermined potential, e.g., a negative potential is applied to the gate electrode 11, such n-type inversion layer disappears so that the lateral power MOS- 40 FET becomes an OFF state.

However, in the conventional lateral power MOSFET shown in FIG. 1, in order to maintain the breakdown voltage between the drain and the source in the OFF state in excess of a predetermined high value, a concentration of the n-type 45 Si drain region 4 must be reduced and a length between the p type Si base region 5 and the high impurity concentration n⁺-type Si drain region 18 must be made longer. As a result, a current path becomes longer and the on-resistance is increased. That is to say, there is in general a trade-off 50 relation between the breakdown voltage and the on-resistance of the power MOSFET.

As well known in the art, in a so-called abrupt junction wherein it is supposed that a high impurity concentration p⁺ type region is connected to an n-type region of relatively low 55 impurity concentration N_d and that a depletion layer is extended only in the n-type region, a breakdown voltage V_B has a relation with an impurity concentration N_d , as expressed by Eq.(1) deduced in compliance with a onedimensional approximation model.

$$N_d = \epsilon E_c^2 / (2qV_B) \tag{1}$$

Where, ϵ is a dielectric constant, q is unit charge, and E_c is a critical electric field. A width W of the depletion layer at breakdown can be expressed by

$$W=2V_B/E_c \tag{2}$$

For contrast, a resistance R_d of a semiconductor region having a unit sectional area and a length W can be given by

$$R_d = W/(qN_d\mu_n)$$
 (3)

Where, μ_n is the electron mobility in bulk of respective semiconductor materials.

Furthermore, in the case of abrupt junction, it has been known that, with respect to Si, relations given by Eqs.(4) and (5) can be derived approximately for the impurity concentration N_d and the depletion-layer width W respectively.

$$N_d$$
=2.01×10¹⁸ $V_B^{-4/3}$ (4)

$$W=2.58\times10^{-6}V_{R}^{7/6} \tag{5}$$

In the conventional example of the lateral power MOS-FET shown in FIG. 1, if the power MOSFET of 200 V class, for instance, is explained as an example, the impurity concentration of the n-type Si drain region 4 becomes 1.7×10^{15} cm⁻³ based on Eq.(4). In addition, as the distance W between the p type Si base region 5 and the high impurity concentration n⁺-type Si drain region 18, 12.5 μ m is needed from Eq.(5). At this time, if the electron mobility μ_n in the Si bulk is assumed to 1340 cm²/V·s, the drain resistance R_d becomes a large value such as $3.4 \times 10^{-3} \Omega$ cm² from Eq.(3). In fact, since other resistances such as a contact resistance are added to the on-resistance of the power MOSFET, the drain resistance R_d becomes a larger value. In other words, once the distance W between the base region and the drain In the lateral power MOSFET shown in FIG. 1, if a 30 region and the impurity concentration N_d in the drain region are defined, a structurally determined breakdown voltage and a correlative value of on-resistance can be derived in the power MOSFET in the prior art, both the breakdown voltage and the on-resistance being insufficient respectively.

SUMMARY OF THE INVENTION

The present invention has been made to overcome the above problems and it is an object of the present invention to provide a power MOSFET which is capable of reducing an on-resistance while maintaining a high breakdown voltage between source and drain regions.

It is another object of the present invention to provide a power MOSFET which is capable of achieving a higher drain voltage by dividing an application of a drain voltage into two sub-drain voltages each having rather smaller

It is still another object of the present invention to provide a method for manufacturing a power MOSFET which is capable of reducing an on-resistance while maintaining a high breakdown voltage between source and drain regions.

It is yet still another object of the present invention to provide a method for manufacturing a power MOSFET which is capable of easily manufacturing a MOSFET having a high breakdown voltage and a low on-resistance.

In order to achieve the above objects, a first aspect of the present invention is that the power MOSFET having a plurality of base regions, source regions formed in the base regions and a drain region formed between the base regions, wherein the drain region has a convex portion and at least a part of the convex portion is formed of wide bandgap semiconductor which has a wider bandgap rather than other portion. More particularly, the power MOSFET of the present invention has a hetero junction consisting of wide bandgap semiconductor and another semiconductor having a bandgap narrower than that of the wide bandgap semiconductor in the drain region.